Printed Pages : 4

EEC-402/EC-403(MTU)

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 131402-130403

Roll No. | | | | | | | | | | |

B. Tech.

(SEM. IV) THEORY EXAMINATION, 2014-15

COMPUTER ARCHITECTURE AND ORGANIZATION

Time : **3** Hours] [Total Marks : **100**

Note : (1) Attempt questions from each section as per instructions.

(2) All questions are compulsory

1 Attempt any FOUR parts of the following : **5x4=20**

(a) Explain gate level design.

(b) Explain briefly the main characteristics of queuing model of computer system.

(c) Explain about the different performance measures used to represent a computer system's performance.

(d) Show how to connect n half adders to form n-bit combinational incrementer whose function is to add one to an n-bit number.

(e) Design a multiplexer to implement a full adder and give explanation.

2 Attempt any FOUR parts of the following : **5x4=20**

(a) Give the internal structure of a CPU.

(b) Draw and explain the architecture of accumulator based CPU.

(c) What is addressing mode? Explain the various types of addressing modes with examples.

(d) List and describe floating point arithmetic instruction of Motorola 680X0 instruction set.

(e) What are the advantages and disadvantages of RISC and CISC?

3 Attempt any TWO parts of the following : **10x2=20**

(a) Explain the Booth algorithm for multiplication. Perform (+15) * (-13) using Booth algorithm. Assume 5-bit registers that hold signed numbers.

(b) Draw a space – time diagram for a six segment pipeline showing the time it takes to process 8 tasks. a non pipeline system takes 50 ns to process a task . The same task can be processed in a six segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 1.00 tasks. What is the maximum speed up that can be achieved?

(c) A computer has 16 registers, an ALU with 32 operations, and a shifter with eight operations, all connected to a common bus system.

(i) Formulate a control word fora micro operation

(ii) Specify number of bits in each field of the control word and give a general encoding scheme.

(iii) Show th bits of control word that specify the micro operation R4 ← R5 ← R6.

4 Attempt any TWO parts of the following : **10x2=20**

(a) Give the IEEE representation for floating point numbers.

(b) Explain vertical and horizontal micro program logic, which is better with respect to programmer.

(c) Design a 4-stage instruction pipeline and show how its performance is improved over the sequential execution.

5 Attempt any TWO parts of the following : **10x2=20**

(a) What are the various mapping techniques used in the cache organization?

(b) Explain the Daisy chaining mechanism for bus arbitration. Analyze the three bus arbitration method – Daisy chaining, polling and independent requesting with respect to communication reliability in the event of hardware failures.

(c) Give the functional block diagram of microprocessor 8085 and explain it in brief.
