Printed Pages : 3

NMCA014

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : **214432**

Roll No. | | | | | | | | | | |

M. C. A.

(SEM. IV) THEORY EXAMINATION, 2014-15

ADVANCED COMPUTER ARCHITECTURE

Time : **3** Hours] [Total Marks : **100**

Note : Attempt **all** questions. **All** questions carry **equal** marks.

1 Attempt any four parts : **5×4=20**

(a) What is m-way interleaving ? Discuss different types of memory interleaving.

(b) Comment on balancing of system bandwidth.

(c) Differentiate between parallel and distributed processing.

(d) Why array computers are termed as parallel computers ?

(e) Discuss static and dynamic dalaflow architecture models in short.

(f) Elaborate Flynn's classification.

2 Attempt any two parts : **10×2=20**

(a) How multi-cache coherence problem is handled ?

(b) Distinguish between :

(i) Medium grain and fine grain multicomputers.

(ii) Single threaded and multithreaded processor architecture.

(c) Give the difference between a thread, a trace and a process. Also explain how simultaneous and multithreading is superior to multitasking.

3 Attempt any two parts : 10×2=20

(a) Explain how DOP and number of processors affect the performance of a parallel computing system ? Discuss various speed up performance laws.

(b) Explain the various types of system performance factors in a parallel architecture.

(c) Discuss various classification of parallel processing mechanisms in uniprocessor computers.

4 Attempt any two parts : 10×2=20

(a) Explain hierarchical memory system. What do you mean by hit ratio and failure ratio ?

(b) Differentiate between super scalar and vector processors.

(c) Discuss various advanced pipelined techniques.

5 Attempt any two parts : 10×2=20

(a) Explain the following terms associated with fast and efficient synchronization schemes on a shared memory multiprocessor.

(i) Busy wait versus sleep wait protocols for sole access of a critical section.

(ii) Post synchronization.

(b) Vectorizing computers generally detect loops that can be executed on a pipelined vector computer. Are the vectorization algorithms used by vectorizing compilers suitable for MIMD machine parallelization ?

(c) Write short notes on :

(i) Combined parallel work sharing constructs.

(ii) Open MP internal control variables.
