(i) Auxiliary memory (ii) Main memory

(iii) Cache memory (iv) Virtual memory

(c) Write short notes on :

(i) Hit (ii) Miss (iii) Hit-ratio

(iv) Write through (v) Write back (vi) Page

(vii) Block (viii) Address space (ix) Memory space

(x) Valid bit

Q5. Attempt any ***two*** parts of the following : 10x2=20

(a) Describe DMA controller and DMA architecture with suitable block diagram.

(b) Explain serial and parallel Bus arbitration technique with suitable diagram.

(c) Explain the interface and how it can communicate with CPU in interrupt initiated transfer mode.

Printed Pages : 4

NMCA215

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 214222

Roll No.

MCA

(SEM. II) THEORY EXAM. 2014-15

COMPUTER ORGANIZATION

Time : 3 Hours] [Total Marks : 100

Note : Attempt the questions as indicated.

Q1. Attempt any ***four*** parts of the following : 5x4=20

(a) Design a full-adder circuit and half-adder circuit using NAND gates only.

(b) Show step by step multiplication process using Booth algorithm, when the following binary numbers are multiplied, (assume 5 bit registers that hold signed number) :
(-13)*(+8)

(c) Simplify the Boolean function in sum of product form by mean of a four variable map. Draw the logic diagram with NAND gate.

$F(A,B,C,D) = \sum(0,2,8,9,10,11,14,15)$

(d) Represent (-307.1875_{10}) in single-precision and double-precision IEEE formats.

(e) Define flip-flop and explain the various types with Truth table.

Q2. Attempt any ***four*** parts of the following : 5x4=20

(a) Design block diagram for a common bus system for four registers and explain in detail.

(b) Show the hardware that implements the following statement :

$xyT_0 + T_1 + y\acute{O}T_2 : AR \leftarrow AR + 1$

(c) What do you understand by addressing modes? Explain at least four.

(d) Write a program to evaluate arithmetical expression using a general register with two and one address instruction

$$X = \frac{(A-E)+C*(D*E-F)}{G+H*K}$$

(e) How stack is implemented in general micro processor system?

Q3. Attempt any ***four*** parts of the following : 5x4=20

(a) Explain the following with suitable steps :

(i) Storing a word into the memory (ii) Fetch a word from the memory

(b) What do you understand by hard wired control logic? Explain with suitable diagram.

(c) Explain micro program sequencer with suitable block diagram.

(d) Explain characteristics of RISC and CISC architecture for microprocessor.

(e) Explain execution of complete instruction with steps.

Q4. Attempt any ***two*** parts of the following : 10x2=20

(a) Explain the following mapping technique for cache memory in detail :

(i) Direct mapping (ii) Set associative mapping

(b) Explain in detail with suitable diagram :