DR. A.P.J. ABDUL KALAM TECHNICAL UNIVERSITY, UTTAR PRADESH, LUCKNOW

Syllabus

For

M.Tech.

VLSI DESIGN

(VLSI & EMBEDED SYSTEM,
ELECTRONICS DESIGN & TECHNOLOGY,
ELECTRONICS CIRCUTICS & SYSTEM DESIGN)

(Effective from the Session: 2016-17)

Dr. A.P.J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow

Study and Evaluation Scheme M. Tech. in VLSI DESIGN

(Effective from Session 2016-17)

First Year, Semester-I

Sr. No.	Course Code	Subject	Periods			Credit	Evaluation Scheme					Subject Total
							Theory			Practical		
			L	T	P		CT	TA	ESE	TA	ESE	
1.	MTVL101	Low Power VLSI Design	3	0	0	3	20	10	70	-	-	100
2.	MTVL102	FPGA Architecture & Applications	3	0	0	3	20	10	70	-	-	100
3.	MTVL01?	Departmental Elective I	3	0	0	3	20	10	70	-	-	100
4.	MTVL02?	Departmental Elective II	3	0	0	3	20	10	70	-	-	100
5.		Research Process & Methodology	3	0	0	3	20	10	70	-	-	100
6.	MTVL151	VLSI Circuit Design Lab	0	0	3	2	-	-	-	20	30	50
7.	MTVL152	FPGA Design Lab	0	0	3	1	-	-	-	20	30	50
		Total	15	0	6	18						600

First Year, Semester-II

Sr. No.	Course Code	Subject	Periods			Credit	Evaluation Scheme					Subject Total
							Theory			Practical		
			L	T	P		CT	TA	ESE	TA	ESE	
1.	MTVL201	Hardware Description Languages	3	0	0	3	20	10	70	-	-	100
2.	MTVL202	VLSI DSP Architectures	3	0	0	3	20	10	70	-	-	100
3.	MTVL03?	Departmental Elective III	3	0	0	3	20	10	70	-	-	100
4.	MTVL04?	Departmental Elective IV	3	0	0	3	20	10	70	-	-	100
5.	MTVL05?	Departmental Elective V	3	0	0	3	20	10	70	-	-	100
6.	MTVL251	Advanced VLSI Design Lab	0	0	3	2	-	-	-	20	30	50
7.	MTVL252	Seminar I	0	0	3	1	-	-	-	50		50
		Total	15		6	18						600

Second Year, Semester-III

Sr. No.	Course Code	Subject	Periods			Credit	Evaluation Scheme					Subject Total
							Theory			Practical		
			L	T	P		CT	TA	ESE	TA	ESE	
1.	MTVL351	Seminar II	0	0	6	3	-	-	-	100	-	100
2.	MTVL352	Dissertation	0	0	30	15	-	-	-	200	300	500
		Total			36	18						600

Second Year, Semester-IV

S. No.	Course Code	Subject	Periods			Credit	Evaluation Scheme					Subject Total
							Theory			Practical		
			L	T	P		CT	TA	ESE	TA	ESE	
1.	MTVL451	Dissertation	0	0	36	18	-	-	-	200	400	600
		Total			36	18						600

Departmental Elective I

MTVL 011: SOC Design
MTVL 012: Designing with ASICS
MTVL 013: Analog VLSI Design

Departmental Elective II

MTVL 021: Advanced Embedded Systems
MTVL 022: Testing of VLSI Circuits
MTVL 023: Digital IC Design

Departmental Elective III

MTVL 031: Advanced Microcontroller & Systems
MTVL 032: VLSI based SignalProcessing Architectures
MTVL 033: Analog IC Design

Departmental Elective IV

MTVL 041: Real Time Operating Systems
MTVL 042: VLSI Testing &Testability
MTVL 043: Memory Technologies

Departmental Elective V

MTVL 051: Algorithms for VLSI Design Automation
MTVL 052: MEMS & Micro Sensor Design
MTVL 053: Embedded System for Wireless Communication

MTVL101 –Low Power VLSI Design

UNIT I: LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II: MOS/BiCMOS PROCESSES: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT III: LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

UNIT IV: DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT V: CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

UNIT VI: LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT VII: LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT VIII: SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

Text Books:

1. Yeo Rofail/ Gohl, CMOS/BiCMOS ULSI low voltage, low power, PearsonEducation.
2. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP.
3. Douglas A.Pucknell& Kamran Eshraghian, Basic VLSI Design, PHI Publication.
4. J.Rabaey, Digital Integrated circuits, PHI Publication.
5. Sung-mo Kang and Yusuf Leblebici, CMOS Digital ICs, TMH Publication .
6. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

MTVL102 –FPGA Architecture & Applications

UNIT-I

Programmable Logic ROM, PLA, PAL, PLD, PGA–Features, programming and applications using complex programmable logic devices Altera series–Max 5000/7000 series and Altera FLEX logic–10000 series CPLD, AMD's–CPLD (Mach 1 to 5); Cypress FLASH 370 Device Technology, Lattice PLST's Architectures–3000 Series–Speed Performance and in system programmability.

UNIT-II

FPGAs Field Programmable Gate Arrays–Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs.

UNIT-III

Case Studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T–ORCA's (Optimized Reconfigurable Cell Array): ACTEL's–ACT-1,2,3 and their speed performance.

UNIT-IV

Finite State Machines (FSM)-I Top-down Design–State Transition Table, state assignments for FPGAs,Problem of initial state assignmentfor one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL.

UNIT-V

Finite State Machines (FSM)-IIAlternative realization for state machine chart using microprogramming.Linked state machines,One–Hot statemachine, Petrinetes for statemachines–basic concepts, properties, Extended petrinetes for parallelcontrollers. Finite State Machine–Case Study, Meta Stability,Synchronization.

UNIT-VI

FSM Architectures and Systems Level Design Architectures centered around non-registered PLDs,State machine designs centered around shift registers,One –Hot design method,Use of ASMs in One –Hot design. K Application of One –Hot method, System level design controller, data path and functional partition.

UNIT-VII

Digital front end Digital Design Tools for (FPGAs & ASICs) using Cadence EDA Tool ("FPGA Advantage") –Design Flow Using FPGAs.

UNIT-VIII

Guidelines and Case Studies Parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

Reference Books:

1. P.K.Chan& S. Mourad, Digital Design using Field ProgrammableGate Array, Prentice Hall.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology,Kluwer Academic Pub.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.
4. S.Brown,R.Francis, J.Rose, Z.Vransic, Field Programmable GateArray,Kluwer Pub.
5. Richard FJinder , "Engineering Digital Design,"Academic press

MTVL201 –Hardware Description Languages

UNIT I**HARDWARE MODELING WITH THE VERILOG HDL :** Hardware Encapsulation –TheVerilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, StructuralConnections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware,Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis,Language Conventions, Representation of Numbers.

UNIT II**LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOGHDL:** User-Defined Primitives, User Defined Primitives – Combinational Behavior User-DefinedPrimitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, LogicValue Set, Data Types, Strings. Constants, Operators, Expressions and Operands, OperatorPrecedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions,Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, VerilogModels for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation,Inertial Delay Effects and Pulse Rejection.

UNIT III**BEHAVIORAL DESCRIPTIONS IN VERILOG HDL:** Verilog Behaviors, BehavioralStatements, Procedural Assignment, Procedural Continuous Assignments, Procedural TimingControls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-BlockingAssignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of SimultaneousProcedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments andAmbiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of DelayConstructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, ModuleContents, Behavioral Models of Finite State Machines.

UNIT IV**SYNTHESIS OF COMBINATIONAL LOGIC:** HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles forSynthesis of Combinational Logic, Technology Mapping and Shared Resources, Three StateBuffers, Three State Outputs and Don t Cares, Synthesis of Sequential Logic Synthesis ofSequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, RegisteredCombinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets,Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

UNIT V**SYNTHESIS OF LANGUAGE CONSTRUCTS:** Synthesis of Nets, Synthesis of RegisterVariables, Restrictions on Synthesis of “X” and “Z”, Synthesis of Expressions and Operators,Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets,Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops,Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-DefinedTasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of CompilerDirectives.

UNIT VI**SWITCH-LEVEL MODELS IN VERILOG:** MOS Transistor Technology, Switch LevelModels of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loadsand Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths,Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of SignalStrengths, Signal Strengths and Wired Logic. Design Examples in Verilog.

UNIT VII**INTRODUCTION TO VHDL:** An Overview of Design Procedures used for System Designusing CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. DesignVerification Tools. Examples using Commercial PC Based on VHDL Elements of VHDL TopDown Design with VHDL Subprograms. Controller Description VHDL Operators.

UNIT VIII**BEHAVIORAL DESCRIPTION OF HARDWARE IN VHDL:** Process Statement AssertionStatements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design.Differences between VHDL and Verilog.

Reference Books:

1. M.D.CILETTI, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice-Hall.
2. Z.NAWABI, VHDL Analysis and Modeling of Digital Systems, McGraw Hill.
3. M.G.ARNOLD, Verilog Digital – Computer Design", Prentice-Hall (PTR).
4. PERRY, "VHDL", McGraw Hill.

MTVL202 –VLSI DSP Architectures

Essential features of Instruction set architectures of CISC, RISC and DSP processors and their implications for Implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor. Assessing understanding performance: Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls.

Data path and control: Introduction, logic design conventions, building a data path, a simple implementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls.

Enhancing performance with pipelining: An overview of pipelining, a pipe lined data path, pipe lined control, data hazards and forwarding, data hazards and stalls, branch hazards, using a hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls

Computational accuracy in DSP implementations: Introduction, number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors.

Architectures for programmable digital signal processing devices: introduction, basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

Text Books:

1. D.A, Patterson, J.L. Hennessy, Computer Organization and Design: Hardware / Software Interface, 4th Edition, Elsevier.
2. A.S. Tannenbaum, Structured Computer Organization, 4th Edition, Prentice-Hall
3. W. Wolf, Modern VLSI Design: Systems on Silicon, 2nd Edition, Pearson Education
4. KeshabParhi, VLSI digital signal processing systems design and implementations, Wiley
5. Avatar Sigh, Srinivasan S, Digital signal processing implementations using DSP microprocessors with examples, Thomson.

MTVL151 – VLSI Circuit Design Lab

Experiments shall be carried out using Tanner/Mentor Graphics/Cadence/Xilinx Tools

Session – I: Digital IC Design Laboratory

1. Introduction to SPICE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis)

2. Modeling of Diodes, MOS transistors, Bipolar Transistors etc using SPICE.

3. An Overview of Tanner EDA Tool/MicroWind/Electric/ Magic/LTSpice

4. I-V Curves of NMOS and PMOS Transistors

5. DC Characteristics of CMOS Inverters (VTC, Noise Margin)

6. Dynamic Characteristics of CMOS Inverters (Propagation Delay, Power Dissipation)

7. Schematic Entry/Simulation/ Layout of CMOS Combinational Circuits

8. Schematic Entry/Simulation/ Layout of CMOS Sequential Circuits

9. High Speed and Low Power Design of CMOS Circuits

Session-II: Analog IC Design Laboratory

1. Study of MOS Characteristics and Characterization

2. Design and Simulation of Single Stage Amplifiers (Common Source, Source Follower, Common Gate Amplifier)

3. Design and Simulation of Single Stage Amplifiers (Cascode Amplifier, Folded Cascode Amplifier)

4. Design and Simulation of a Differential Amplifier (with Resistive Load, Current Source Biasing)

5. Design and Simulation of Basic Current Mirror, Cascode Current Mirror

6. Analysis of Frequency response of various amplifiers (Common Source, Source Follower, Cascode, Differential Amplifier

7. Design/Simulation/Layout of Telescopic Operational Amplifier/ Folded Cascode Operational Amplifier

MTVL152 –FPGA Design Lab

Modeling and Functional Simulation of the following digital circuits (with Xilinx/ ModelSim tools) using VHDL/Verilog Hardware Description Languages

1. Part – I Combinational Logic: Basic Gates, Multiplexer, Comparator, Adder/ Substractor, Multipliers, Decoders, Address decoders, parity generator, ALU

2. Part – II Sequential Logic: D-Latch, D-Flip Flop, JK-Flip Flop, Registers, Ripple Counters, Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial), Cyclic Encoder / Decoder.

3. Part – III Memories and State Machines: Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Arithmetic Multipliers using FSMs

4. Part-IV: FPGA System Design: Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation of UART/Mini Processors on FPGA/CPLD etc

MTVL251 – Advanced VLSI Design Lab

Session-I: VLSI System Design

1. Design/Simulation of other analog building blocks
a. Comparators
b. Oscillators
c. PLLs
d. switched capacitor circuits
e. Noise Analysis

2. Mini Projects involving
a. Unpipelined MIPS Processor
b. Pipelined MIPS Processor
c. Out of Order Execution with Tomasulo's Algorithm
d. Communication Controllers
e. Arithmetic Circuits
f. DSP Systems

Session-II: ASIC Design

Experiments shall be carried out using Mentor Graphics/Cadence Tools

1. Part-I: Backend Design

Schematic Entry/ Simulation / Layout/ DRC/PEX/Post Layout Simulation of CMOS Inverter, NAND Gate, OR Gate, Flip Flops, Register Cell, Half Adder, Full Adder Circuits

2. Part-II: Semicustom Design

HDL Design Entry/ Logic Simulation, RTL Logic Synthesis, Post Synthesis Timing Simulation, Place & Route, Design for Testability, Static Timing Analysis, Power Analysis of Medium Scale Combinational, Sequential Circuits

3. Part-III: High Speed/Low Power CMOS Design

Designing combinational/sequential CMOS circuits for High Speed

Designing combinational/sequential CMOS circuits for Low Power

MTVL011 –SOC Design

Motivation for SoC Design - Review of Moore's law and CMOS scaling, benefits of system-on-chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System-on-Chip, and System-in-Package. Typical goals in SoC design – cost reduction, powerreduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.

System On Chip Design Process: A canonical SoC Design, SoCDesignflow, waterfall vs spiral, top down vs bottom up, Specification requirement, Types of Specification, System Design Process, System level design issues, Soft IP vs Hard IP, IP verification and Integration,

Hardware-Software codesign, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc.

Embedded Memories –cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence.MESI protocol and Directory-based coherence.

Interconnect architectures for SoC. Bus architecture and its limitations. Network on Chip (NOC) topologies.Mesh-based NoC.Routing in anNoC.Packet switching and wormhole routing.

MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design

Case Study: A Low Power Open Multimedia Application Platform for 3G and 4G Wireless Communication Technology.

Text Books:

1. SudeepPasricha and NikilDutt,"On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers.
2. Rao R. Tummala, MadhavanSwaminathan, "Introduction to system on package sop-Miniaturization of the Entire Syste", McGraw-Hill Publication.
3. James K. Peckol, "Embedded Systems: A Contemporary Design Tool", Wiley Student Edition.
4. Michael Keating, Pierre Bricaud, "Reuse Methodology Manual for System on Chip designs", Kluwer Academic Publishers, 2nd edition, 2008.
5. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits", Tata McGraw-Hill Publication.

MTVL012 –Designing with ASICs

Types of ASICs – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers.

ASIC Library design: Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC.

Low level design entry: Schematic entry – low level design languages – PLA tools – EDIF – An overview of VHDL and verilog.

Logic synthesis in verilog and & VHDL simulation.

ASIC Construction – Floor planning & placement – Routing.

Text / References:

1. J.S. Smith, "Application specific Integrated Circuits", Addison Wesley, 1997.

MTVL013 –Analog VLSI Design

Introduction to Analog VLSI

Analog integrated circuit design, Circuit design consideration for MOS challenges in analogcircuit design, recent trends in analog VLSI circuits.

Analog MOSFET Modeling

MOS transistor, Low frequency MOSFET Models, High frequency MOSFET Models, temperature effects in MOSFET, Noise in MOSFET.

Current Source, Sinks and References

MOS Diode/Active resistor, Simple current sinks and mirror, Basic current mirrors, advancecurrent mirror, Current and Voltage references, bandgap references.

CMOS Amplifier

Performances matrices of amplifier circuits, Common source amplifier, Common gate amplifier,Cascode amplifier, Frequency response of amplifiers and stability of amplifier.

CMOS Feedback Amplifier

Feedback equation, Properties of negative feedback on amplifier design, Feedback Topology,Stability.

CMOS Differential Amplifier

Differential signalling, source coupled pair, Current source load, Common mode rejection ratio,CMOS Differential amplifier with current mirror load,, Differential to single ended conversion.

CMOS Operational amplifier

Block diagram of Op-amplifier, Ideal characteristics of Op-Amplifier, Design of two stage Op-Amplifier, Compensation of Op-Amplifier, Frequency response of Op-Amplifier, OperationalTransconductance Amplifier (OTA).

CMOS Comparator

Characteristic of a comparator, Two stage open loop comparator, Special purpose comparator,Regenerative comparator, High output current amplifier, High speed comparator.

Switched Capacitor Circuits

Switched capacitor circuits, Switched capacitor amplifiers, Switch capacitor integrators.

Text Book:

1. BehzadRazavi , “Design of Analog CMOS Integrated Circuits”, McGraw Hill Publication.
2. R. Jacob Baker, Harry W. Li, and David E. Boyce,“CMOS: Circuit Design , Layout and Simulation”, Prentice Hall of India
3. David A. Johns and Ken Martin, “Analog Integrated circuit Design, John Wiley & Sons.

MTVL021 –Advanced Embedded Systems

Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware,Other System Components.

Characteristics and Quality Attributes of Embedded Systems: Hardware Software Co-Design and Program Modeling: Fundamental Issues inHardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware SoftwareTrade-offs.

Embedded Hardware Design and Development :EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port, junction,creating part numbers, Design Rules check, Bill of materials, Netlist creation , PCB Layout Design – Building blocks, Component placement,PCB track routing.

ARM -32 bit Microcontroller family. Architecture of ARM Cortex M3 –General Purpose Registers, Stack Pointer, Link Register, ProgramCounter, Special Register,.Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. AdvancedProgramming Features.Memory Protection. Debug Architecture.

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages

Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads,Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, TaskSynchronization, Device Drivers, How to Choose an RTOS.

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Crosscompilation, Disassembler/ELDompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

Text Books:

1. Shibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Ltd
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, Newnes, (Elsevier).
3. James K Peckol, “Embedded Systems – A contemporary Design Tool”, John Weily& Sons.

MTVL022 –Testing of VLSI Circuits

UNIT I - BASICS OF TESTING AND FAULT MODELING

Introduction- Principle of testing - types of testing - DC and AC parametric tests - fault modeling - Stuck-at fault - fault equivalence - fault collapsing - fault dominance - fault simulation

UNIT II - TESTING AND TESTABILITY OF COMBINATIONAL CIRCUITS

Test generation basics - test generation algorithms - path sensitization - Boolean difference – D-algorithm – PODEM - Testable combinational logic circuit design.

UNIT III - TESTING AND TESTABILITY OF SEQUENTIAL CIRCUITS

Testing of sequential circuits as iterative combinational circuits - state table verification - test generation based on circuit structure - Design of testable sequential circuits - Ad Hoc design rules - scan path technique (scan design) - partial scan - Boundary scan

UNIT IV - MEMORY, DELAY FAULT AND IDDQ TESTING

Testable memory design - RAM fault models - test algorithms for RAMs – Delay faults - Delay test- IDDQ testing - testing methods - limitations of IDDQ Testing

UNIT V - BUILT-IN SELF-TEST

Test pattern generation of Built-in Self-Test (BIST) - Output response analysis – BIST architectures.

Reference Books:

1. P. K. Lala, “Digital Circuit Testing and Testability”, Academic Press.
2. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwar Academic Publishers.
3. N.K. Jha and S.G. Gupta, “Testing of Digital Systems”, Cambridge University Press.
4. ZainalabeNavabi, “Digital System Test and Testable Design: Using HDL Models and Architectures”, Springer.

MTVL023 –Digital IC Design

UNIT-I Introduction: Historical Perspective, Issues in Digital Integrated Circuit Design, Quality Metrics of a Digital Design - Cost of an Integrated Circuit, Functionality and Robustness, Performance, Power and Energy Consumption – The Manufacturing Process - Introduction, Manufacturing CMOS Integrated Circuits, The Silicon Wafer, Photolithography, Some Recurring Process Steps Simplified CMOS Process Flow, Design Rules — The Contract between Designer and Process Engineer

UNIT-II Devices: Introduction, The Diode, A First Glance at the Diode — The Depletion Region, Static Behavior, Dynamic, or Transient, Behavior, The Actual Diode—Secondary Effects, The SPICE Diode Model, The MOS(FET) Transistor, A First Glance at the Device, The MOS Transistor under Static Conditions, Dynamic Behavior, The Actual MOS Transistor—Some Secondary Effects, SPICE Models for the MOS Transistor – **Wire:** Introduction, A First Glance, Interconnect Parameters — Capacitance, Resistance, and Inductance, Capacitance, Resistance, Inductance

UNIT-III The CMOS Inverter: Introduction, The Static CMOS Inverter — An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Switching Threshold, Noise Margins, Robustness Revisited, Performance of CMOS Inverter: The Dynamic Behavior, Computing the Capacitances, Propagation Delay: First-Order Analysis, Propagation Delay from a Design Perspective, Power, Energy, and Energy-Delay, Dynamic Power Consumption, Static Consumption, Perspective: Technology Scaling and its Impact on the Inverter Metrics

UNIT-IV Designing Combinational Logic Gates in CMOS: Introduction, Static CMOS Design, Complementary CMOS, Ratioed Logic, Pass-Transistor Logic, Dynamic CMOS Design, Dynamic Logic: Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Perspectives, How to Choose a Logic Style, Designing Logic for Reduced Supply Voltages

UNIT-V Designing Sequential Logic Circuits: Introduction, Timing Metrics for Sequential Circuits, Classification of Memory Elements, Static Latches and Registers, The Bistability Principle, Multiplexer-Based Latches Master-Slave Edge-Triggered Register, Low-Voltage Static Latches, Static SR Flip-Flops—Writing Data by Pure Force, Dynamic Latches and Registers, Dynamic Transmission-Gate Edge-triggered Registers C2MOS—A Clock-Skew Insensitive Approach, True Single-Phase Clocked Register (TSPCR), Pipelining: An approach to optimize sequential circuits, Latch- vs. Register-Based Pipelines, NORA-CMOS—A Logic Style for Pipelined Structures, Non-Bistable Sequential Circuits, The Schmitt Trigger, Monostable Sequential Circuits, Astable Circuits, Perspective: Choosing a Clocking Strategy

Reference Books:

1. Jan M. RabaeyAnanthaChandrakasan, &BorivojeNikolic, “Digital Integrated Circuits – A design perspective”, PHI Publication.
2. S. M. Kang & Y. Leblebici, “CMOS Digital Integrated Circuits”, McGraw Hill Publication.
3. Jackson & Hodges, “Analysis and Design of Digital Integrated circuits”,. TMH Publication.
4. Ken Martin, “Digital Integrated Circuit Design”, Oxford Publications.
5. Sedra and Smith, “Microelectronic Circuits” Oxford Publications.

MTVL031 –Advanced Microcontrollers and Systems

Motivation for advanced microcontrollers – Low Power embedded systems, On-chip peripherals, low-power RF capabilities. Applications of Microcontrollers.

MSP430 – 16-bit Microcontroller family. CPU architecture, Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus – architecture. The assembly language and „C programming for MSP-430 microcontrollers.On-chip peripherals. WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC), ADC, DAC, Digital I/O. Using the low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and interrupts.

ARM -32 bit Microcontroller family. Architecture of ARM Cortex M3 – General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming.Advanced Programming Features.Memory Protection. Debug Architecture.

Applications – Wireless Sensor Networking with MSP430 and Low-Power RF circuits; Pulse Width Modulation(PWM) in Power Supplies.

Reference Books:

1. Joseph Yiu, " The Definitive Guide to the ARM Cortex-M3, , Newnes, (Elsevier).
2. John Davies, " MSP430Microcontorller Basics",Newnes (Elsevier Science).
3. MSP430 Teaching CD-ROM, Texas Instruments.

MTVL032 –VLSI based Signal Processing Architectures

Introduction for DSP algorithms: VLSI Design flow, Mapping algorithms intoArchitectures: Graphical representation of DSP algorithms – signal flow graph (SFG), dataflow graph (DFG), critical path, dependence graph (DG). Data path synthesis, controlstructures, Optimization at Logic Level and architectural Design, Loop bound and iterationbound, Algorithms for computing iteration bound, Iteration bound of Multirate data-flowgraphs.

Parallel and pipeline of signal processing application : Architecture for real timesystems, latency and throughput related issues, clocking strategy, power consciousstructures, array architectures; Pipelining processing of Digital filter**,** Parallel processing**,**Parallel and pipelining for Low power design**,** Optimization with regard to speed, area andpower, asynchronous and low power system design, ASIC (application specific integratedcircuits) and ASISP application specific instruction set processors) design.

Systolic Array Architecture: Methodology of systolic array architecture**,** FIR basedSystolic Array**,** Selection of Scheduling Vector**,** Matrix multiplication of systolic array.

Architecture of different signal processing modules: Convolution technique, Retimingconcept, Folding /Unfolding Transformation, CORDIC architecture.

Low power Design: Theoreticalbackground, Scaling v/s power consumption, poweranalysis, Power reduction techniques, Power estimation approach.

Application in communication and signal processing system: Transformationarchitectures**,** source and channel coding structures**,** Motion Estimation and motioncompensation for video**,** Speech processing algorithm.

Reference Books:

1. K.K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, John Wiley & Sons Publication
2. Richard J, Higgins, Digital Signal Processing in VLSI, Prentice Hall Publication.
3. M.A. Bayoumi, VLSI Design Methodology for DSP Architectures, Kluwer Academic Press.
4. U. Meyer – Baese , Digital Signal Processing with FPGAs, Springer Publications.

MTVL033 –Analog IC Design

UNIT I

Basic MOS Device Physics: General Considerations, MOSFET as a Switch, MOSFET Structure, MOS Symbols, MOS I/V Characteristics, Threshold Voltage, Derivation of I/V Characteristics, Second-Order Effects, MOS Device Models, MOS Device Layout, MOS Device Capacitances, MOS Small-Signal Model, MOS SPICE models, NMOS versus PMOS Devices, Long-Channel versus Short-Channel Devices.

UNIT II

Single-Stage Amplifiers, Basic Concepts , Common-Source Stage, Common-Source Stage with Resistive Load ,CS Stage with Diode-Connected Load, CS Stage with Current-Source Load, CS Stage with Triode Load, CS Stage with Source Degeneration, Source Follower, Common-Gate Stage, Cascode Stage, Folded Cascode, Choice of Device Models.

UNIT III

Differential Amplifiers, Single-Ended and Differential Operation. Basic Differential Pair, Qualitative Analysis, Quantitative Analysis, Common-Mode Response, Differential Pair with MOS Loads, Gilbert Cell, Passive and Active Current Mirrors, Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors, Large-Signal Analysis, Small-Signal Analysis, Common-Mode Properties

UNIT IV

Frequency Response of Amplifiers, General Considerations, Miller Effect, Association of Poles with Nodes, Common-Source Stage, Source Followers, Common-Gate Stage, Cascode Stage, Differential Pair **Feedback** General Considerations, Properties of Feedback Circuits, Types of Amplifiers, Feedback Topologies, Voltage-Voltage Feedback, Current-Voltage Feedback, Voltage-Current Feedback, Current-Current Feedback, Effect of Loading, Two-Port Network Models, Loading in Voltage-Voltage Feedback, Loading in Current-Voltage Feedback, Loading in Voltage-Current Feedback, Loading in Current-Current Feedback, Summary of Loading Effects, Effect of Feedback on Noise

UNIT V

Operational Amplifiers, General Considerations , Performance Parameters, One-Stage Op Amps, Two-Stage Op Amps , Gain Boosting , Comparison , Common-Mode Feedback . Input Range Limitations, Slew Rate, Power Supply Rejection. Stability and Frequency Compensation General Considerations, Multipole Systems, Phase Margin, Frequency Compensation, Compensation of Two-Stage Op Amps, Slewing in Two-Stage Op Amps, Other Compensation Techniques.

Reference Books:

1. B. Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill Publications/

2. P. R. Gray & R. G. Meyer, “Analysis and Design of Analog Integrated Circuits”, John Wiley Publications.
3. R. Gregorian and Temes, “Analog MOS Intgrated Circuits for Signal Processing”, Wiley Publications.
4. Ken Martin, “Analog Integrated Circuit Design”, Wiley Publications.
5. Sedra and Smith, “Microelectronic Circuits”, Oxford Publications.
6. B.Razavi, “Fundamentals of Microelectronics”, Wiley Publications.

MTVL041 –Real Time Operating Systems

Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems.

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Reentrant Functions.

Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies.

I/O Resources: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.

Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems.

Multi-resource Services: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion

Soft Real-Time Services: Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services.

Embedded System Components: Firmware components, RTOS system software mechanisms, Software application components.

Debugging Components: Exceptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics, External test equipment, Application-level debugging.

Performance Tuning: Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and Call frequency, Fundamental optimizations.

High availability and Reliability Design: Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design tradeoffs, Hierarchical applications for Fail-safe design.

Design of RTOS – PIC microcontroller.

Reference Books:

1. Sam Siewert, “Real-Time Embedded Systems and Components”, Cengage Learning India.
2. MykePredko, “Programming and Customizing the PIC microcontroller”, TMH Publication.
3. Programming for Embedded Systems, Dreamtech Software Team, Jhon Wiley, India

MTVL042 –VLSI Testing and Testability

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing.

VLSI Testing Process and Test Equipment: How to Test Chips? Automatic Test Equipment, Electrical Parametric Testing. Faults in Digital Circuits: Failures and Faults, Modeling of Faults, Temporary Faults.

Test Generation for Combinational Logic Circuits: Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits. Testable Combinational Logic Circuit Design: The Reed-Mullar Expansion Technique, Three-Level OR-AND-OR Design, Automatic Synthesis of Testing Logic, Testable Design of Multilevel Combinational Circuits, Synthesis of Random Pattern Testable Combinational Circuits, Path Delay Fault Testable Combinational Logic Design, Testable PLA Design.

Test Generation for Sequential Circuits: Testing of Sequential Circuits as Iterative Combinational Circuits, State Table Verification, Test Generation Based on Circuit Structure, Functional Fault Models, Test Generation Based on Functional Fault Models.

Design of Testable Sequential Circuits: Controllability and Observability, Ad Hoc Design Rules for Improving Testability, Design of Dignosable Sequential Circuits, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random

Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Nonscan Techniques, Cross Check, Boundary Scan.

Built-In Self-Test: Test Pattern Generation for BIST, Output Response Analysis, Circular BIST, BIST Architectures.

Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs, Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.

Text Books:

1. P. K. Lala, “Digital Circuit Testing and Testability”, Academic Press.
2. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwar Academic Publishers.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House.

MTVL043 –Memory Technologies

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOl, Advanced SRAM Architectures, Application Specific SRAMs; DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM.

Non-Volatile Memories: High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories.

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM Fault Modeling, Electrical Testing, Pseudo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling and Testing, IDDQ Fault Modeling and Testing, Application Specific Memory Testing.

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.

Reference Books:

1. Ashok K. Sharma, “Semiconductor Memories: Technology, Testing and Reliability", Prentice- Hall of India Private Limited.
2. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience Publication.
3. Wen C. Lin, “Handbook of Digital System Design”, CRC Press.
4. KiyooItoh, “VLSI memory chip design”, Springer International Edition.
5. Chenming C Hu, “Modern Semiconductor Devices for Integrated Circuits”, Prentice Hall.

MTVL051 –Algorithms for VLSI Design Automation

VLSI physical design automation and Fabrication VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices

VLSI automation Algorithms Partitioning: Problem formulation, classification ofpartitioning algorithms, Group migration algorithms, simulated annealing.

Floor planning & pin assignment: Problem formulation, classification of floorplanning algorithms, constraint based floor planning, floor planning algorithms for mixedblock& cell design, chip planning, pin assignment, problem formulation, classificationof pin assignment algorithms, General & channel pin assignment Placement Problemformulation, classification of placement algorithms, simulation base placementalgorithms, recent trends in placement

Global Routing and Detailed routing: Problem formulation, classification of global routingalgorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms,performance driven routing Detailed routing problem formulation, classification ofrouting algorithms, introduction to single layer routing algorithms, two layer channelrouting algorithms, greedy channel routing, switchbox routing algorithms.

Over the cell routing & via minimization: Two layers over the cell routers,constrained& unconstrained via minimization

Compaction: Problem formulation, classification of compaction algorithms, onedimensionalcompaction, two dimension based compaction, hierarchical compaction

Reference Books :

1. NaveedShervani, “Algorithms for VLSI physical design Automation”, KluwerAcademic Publisher, Second edition.
2. ChristophnMeinel& Thorsten Theobold, “Algorithm and Data Structures for VLSIDesign”, Kluwer Academic Publisher.
3. R. Drechsler, “Evolutionary Algorithm for VLSI CAD”, Kluwer Academic Publication.

MTVL052 –MEMS & Micro Sensor Design

Introduction to MEMS

MEMS Fabrication Technologies, Materials and Substrates for MEMS, Processes forMicromachining, Characteristics, Sensors/Transducers, Piezoresistance Effect,Piezoelectricity, Piezoresistive Sensor.

Mechanics of Beam and Diaphragm Structures

Stress and Strain, Hooke's Law. Stress and Strain of Beam Structures: Stress, Strain in aBent Beam, Bending Moment and the Moment of Inertia, Displacement of BeamStructures Under Weight, Bending of Cantilever Beam Under Weight.

Air Damping

Drag Effect of a Fluid: Viscosity of a Fluid, Viscous Flow of a Fluid, Drag ForceDamping, The Effects of Air Damping on Micro-Dynamics. Squeeze-film Air Damping:Reynolds' Equations for Squeeze-film Air Damping, Damping of Perforated ThickPlates. Slide-film Air Damping: Basic Equations for Slide-film Air Damping,Couette-flow Model, Stokes-flow Model.

Electrostatic Actuation

Electrostatic Forces, Normal Force, Tangential Force, Fringe Effects, ElectrostaticDriving of Mechanical Actuators: Parallel-plate Actuator, Capacitive sensors. Step and Alternative Voltage Driving: Step Voltage Driving, Negative SpringEffect and Vibration Frequency.

Thermal Effects

Temperature coefficient of resistance, Thermo-electricity, Thermocouples, Thermal andtemperature sensors.

Applications of MEMS in RF

MEMS Resonator Design Considerations, One-Port Micromechanical ResonatorModeling Vertical Displacement Two-Port Microresonator Modeling,Micromechanical Resonator Limitations.

Reference Books:

1. S.M. Sze, “Semiconductor Sensors”, John Wiley & Sons Inc., Wiley Interscience Pub.
2. M.J. Usher, “Sensors and Transducers”, McMillian Hampshire.
3. RS Muller, Howe, Senturia and Smith, “Micro sensors”, IEEE Press.

MTVL053 –Embedded System for Wireless & Mobile Communication

Introduction to wireless technologies: WAP services, Serial and Parallel Communication, Asynchronous and synchronous Communication, FDM,TDM, TFM, Spread spectrum technology.

Introduction to Bluetooth: Specification, Core protocols, Cable replacement protocol

Bluetooth Radio: Type of Antenna, Antenna Parameters, Frequency hoping

Bluetooth Networking: Wireless networking, wireless network types, devices roles and states, adhoc network, scatter net Connection establishment procedure, notable aspects of connection establishment, Mode of connection, Bluetooth security, Security architecture, Security level of services, Profile and usage model: Generic access profile (GAP), SDA, Serial port profile,

Secondary bluetooth profile Hardware: Bluetooth Implementation, Baseband overview, packet format, Transmission buffers, Protocol Implementation: Link Manager Protocol, Logical Link Control Adaptation Protocol, Host control Interface, Protocol Interaction with layers

Programming with Java: Java Programming, J2ME architecture, Javax. bluetooth package Interface, classes, exceptions, Javax. obex Package: interfaces, classes

Bluetooth services registration and search application, bluetooth client and server application.

Overview of IrDA, HomeRF, Wireless LANs, JINI

Reference Books:

1. C.S.R. Prabhu and A.P. Reddi,“ Bluetooth Technology”, PHI Publication.
2. U. Dalal& M. Shukla, "Wireless & Mobile Communication", Oxford University Press.
3. C. Y. William, Lee, "Mobile communication engineering theory and applications", TMH, Publication.
4. S .Haykins, “Communication Systems”, John Wiley and Sons.