B. Tech.

(SEM. VIII) EXAMINATION. 2006-07

VLSI FOR TELECOMMUNICATION

Time : 3 Hours] [Total Marks : 100

Note : (1) Attempt all questions.
(2) All questions carry equal marks.
(3) In case of numerical problems assume suitable data wherever not provided.
(4) Be precise in your answer.

1 Attempt any four parts of the following : \(5 \times 4 = 20\)

(a) Explain the following terms with respect to CMOS chip design hierarchy, regularity, modularity and locality. Give example of each.

(b) Nand implementation is preferred over NOR for CMOS VLSI design. Comment giving suitable example.

(c) Explain the flow for designing of Integrated circuits. What are different hardware design methodologies ? Explain.

(d) Discuss the critical path approach for designing high-speed MOS circuits.

(e) Discuss the effect of channel dimensions on the performance of CMOS transistor.

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(f) Discuss the implications of mixed signal chip design.

2 Attempt any four parts of the following: 5x4=20

(a) What is SPICE? Explain at least two Spice commands each for AC, DC and transient analysis of circuits.

(b) Differentiate between signals and variables with respect to VHDL. What are different assignment statements to define them inside and outside process statement.

(c) Define the following terms with respect to VHDL/VLSI:
   (i) Functional simulation
   (ii) Gate-level simulation
   (iii) Post layout simulation.
   Give at least one example of each.

(d) Discuss with example, Euler-path method for minimum area layout design.

(e) List the various parasitic capacitances associated with a routed CMOS inverter.
   How the net gate capacitance is calculated?

(f) Discuss one CAD tool for VLSI Design in brief.

3 Attempt any two parts of the following: 10x2=20

(a) Design a two input NAND gate in domino logic:
   (i) Draw a transistor schematic
   (ii) Draw a stick diagram.

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(b) Discuss various methods to be used to optimize the switching activity in CMOS integrated circuits.

(c) Draw stick diagram and layout for the following circuit.

![Circuit Diagram]

**Fig. 1**

4 Attempt any two parts of the following:

(a) Discuss the two-phase, non-overlapping clock generation.

(b) Explain the basic block diagram of RF receiver front end. How trade off between Noise and power is achieved at high RF.

(c) Explain what you mean by image compression? Discuss various algorithms.

5 Write short notes on any two parts of the following:

(a) Adaptive filters and equalizers

(b) Video conferencing

(c) Digital audio compression.